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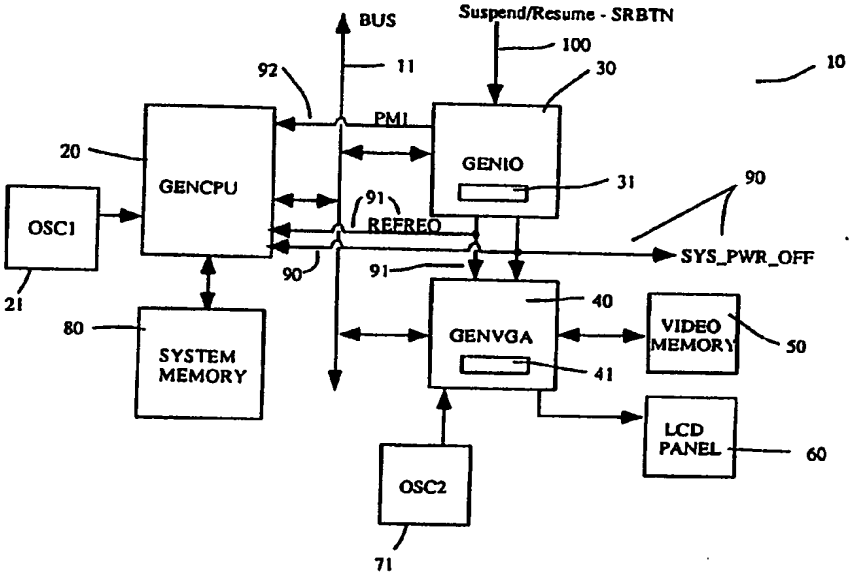
(54) Title: SLOW MEMORY REFRESH IN A COMPUTER WITH A LIMITED SUPPLY OF POWER

(57) Abstract

A power suspend mode activates a slow DRAM refresh in a computer system (10) with a limited source of power. The power suspend (100) mode reduces the power consumed by the computer system (10) while preserving the contents of memory. The cyclic refresh of DRAM (80) using a slow refresh clock substantially reduces the power consumed while the computer is suspended. This technique is particularly useful for battery powered portable computer systems. When an external or internal condition causes the computer system to transition to a power down mode, an IO subsystem (30) notifies the CPU (20) which sets control bits in the IO (30) subsystem and a video subsystem (40). The IO subsystem (30) then begins to generate a slow DRAM refresh pulse (91). Once the CPU (20) and video subsystem (40) sense the power suspend mode activation, the system memory (80) and video memory (50) are refreshed using the slow refresh clock. The power consumed during the refresh process is thereby greatly reduced. When a resume signal is received by the IO subsystem (30), the slow refresh clock (91) is terminated and the system memory (80) and video memory (50) are again refreshed using a normal faster clock.



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SLOW MEMORY REFRESH IN A COMPUTER WITH A LIMITED SUPPLY OF POWER

FIELD OF THE INVENTION

This invention relates to the field of computer architecture, and particularly to a method and apparatus for providing a slow memory refresh in a computer with a limited supply of power.

BACKGROUND OF THE INVENTION

Reducing power consumption is an important issue in many modern personal computers. This issue is particularly important for battery-powered lap-top or notebook style portable computers. Other computers with a limited supply of power also need to be designed with a concern for power conservation. Computers with a limited supply of power are often those designed to be portable. In order to achieve the portability of these computer systems, the power consumed by the system components must be minimized. Reduced power consumption prolongs the battery life and thus increases the feasibility of the computer as a portable system. Clearly, the simplest way to conserve power is to shut the system down entirely; however, shutdown destroys the contents of memory and forces the user to restart and re-boot the computer from scratch. A better method is to provide a reduced power mode which supplies a minimal level of power to vital subsystems thereby saving the processing state of the computer.

Many of these portable computers include a memory subsystem for storing data and instructions for the processor and a video subsystem for storing and displaying a video image on a display screen. The memory subsystem and a video memory in the video subsystem may be configured using dynamic random access memory (DRAM) devices for storing information. DRAMs require a cyclic refresh signal supplied by the computer system in order to prevent the information stored in DRAM from being destroyed. It is advantageous to implement a reduced power

mode wherein the operation of the computer is suspended, but the memory subsystem and video memory is saved. In this way, the computer user may reactivate the system after a suspended period and obtain the same system state and display as present prior to the suspension.

Several systems and methods exist in the prior art for providing a reduced power mode in a computer with a limited source of power. One such system saves the contents of system memory and video memory on a hard disk or a non-volatile memory prior to removing power from the system. This method has several disadvantages. First, the computer system must be configured with a hard disk or non-volatile memory resource. A particular computer may not be so configured. Also, a hard disk or non-volatile memory is an expensive component which raises the overall cost of the system. Secondly, the disk access necessary for saving and restoring memory is a relatively slow operation. There may be a delay in response to the entry and return from the suspend mode. Thirdly, if the suspend mode is entered as a result of a low battery condition, there may not be enough power to access the disk. Disk access is a relatively power intensive operation.

Other systems providing a reduced power mode in a computer with a limited source of power implement such a mode by using static RAM (SRAM) or pseudo static RAM (PSRAM) for system and video memory. SRAM does not require a cyclic refresh signal as required by DRAM. SRAM can therefore operate at a low power consumption rate during a suspend mode without losing data. PSRAM must be put into a standby mode in order to operate the device without refresh. Unfortunately, SRAMs are substantially more expensive than DRAMs. Thus, the overall system cost increases and the competitiveness of the computer system in the marketplace decreases.

Still other systems implement a video memory save operation where the video memory contents are saved in a system memory area. This technique, however, does not reduce the power consumption in the

computer system. If system memory is DRAM, the system memory must still be refreshed during a suspend mode. If system memory is SRAM or some form of non-volatile memory, the system cost increases as mentioned above. In addition, such systems may require additional system memory in order to have enough space to hold the contents of video memory during a power suspend mode. Additional software may also be required to control the allocation and maintenance of system memory used to hold video memory during suspend mode. This additional software may lead to a specially configured BIOS thereby reducing the general applicability of the BIOS supplied with a basic system.

A better computer system design is needed for implementing a more efficient and less expensive power suspend mode.

SUMMARY OF THE INVENTION

The present invention provides a power suspend mode with a slow DRAM refresh in a computer system with a limited source of power. The power suspend mode reduces the power consumed by the computer system while preserving the contents of memory. The cyclic refresh of DRAM using a slow refresh clock substantially reduces the power consumed while the computer is suspended.

The present invention is particularly adapted for use in connection with a microprocessor-based chip set for use in battery-powered personal computers, especially computers of the "notebook" or "laptop" variety. Such a chip set includes a CPU chip, an I/O chip, and typically, a graphics chip.

During a power suspended state, the processor and/or other system devices may be effectively shut down during periods of non-use and then re-started without the need to go through a power up routine. This function is particularly useful in connection with battery-powered computers where power conservation is a primary concern. A key feature of the present invention is that the system may be powered down and later brought back to the same point in an application program at which it was left. Thus, for example, if a computer operator is interrupted while working with an application program, the system can suspend power to conserve battery life. When the operator returns to use the system, it is restored to the same point in the application program as if the system had been running throughout the intervening period of time. The operator need not take any action to save application program results prior to the interruption, nor need the operator take any action to reload the application program when returning to use the computer.

In order to resume the operation of the computer after suspension without the need for re-booting or executing a power up routine, the contents of memory is preserved throughout the power suspension period.

Since DRAM is used in the computer system of the present invention, a significant level of power is required to periodically refresh the contents of DRAM even while suspended. In order to minimize the consumption of power during the DRAM refresh operation, the cyclic refresh of DRAM is slowed to a minimal rate while the computer is suspended thereby substantially reducing the power necessary for preserving the contents of memory.

The computer system of the preferred embodiment comprises a GENCPU (central processing unit) subsystem, an GENIO (input/output) subsystem, and a GENVGA video subsystem. These subsystems are coupled by a data bus. A system memory is coupled to the CPU and a video memory is coupled to the video subsystem. Both the system memory and the video memory comprise low cost DRAM devices requiring a periodic refresh. During normal operations in the preferred embodiment, the video DRAM is refreshed using a 48 MHz clock. System DRAM is refreshed during normal operations using a 16 MHz clock.

The power suspend mode is initiated by the occurrence of an external or internal event and the execution of a suspend instruction by the CPU. Once the suspend instruction is executed, the CPU signals the IO subsystem and the video subsystem of the pending request for suspension by asserting two control bits. One control bit is associated with the video subsystem; the other control bit is associated with the IO subsystem. When the IO subsystem senses the assertion of its associated control bit, GENIO asserts a system power off signal which is received by the video subsystem, GENCPU and other components of the computer system. The pins connecting the CPU, the IO subsystem and the video subsystem to the bus are set to a tri-state (i.e. high impedance) condition which effectively disables communication over the bus. At nearly the same time, the IO subsystem begins sending a slow (32 KHz) clock signal to the CPU and the video subsystem. After the CPU sets the two control bits, the CPU begins to use the slow clock for refreshing the system

DRAM. As a result of the assertion of the video subsystem suspend control bit and the system power off signal, the video subsystem begins using the slow clock for refreshing the video DRAM. Other non-essential components are shut down following the activation of the system power off signal.

When the IO subsystem receives a resume signal as a result of some user or system action, GENIO disables the system power off signal and enables its communication with the bus by removing the tri-state condition. Similarly, GENVGA and GENCPU enable bus communication by removing the tri-state condition on the bus interface. When the CPU senses the deactivation of the system power off signal, a CPU reset is generated, a resume instruction is executed, the system state is restored. The CPU then deactivates the suspend control bits associated with the IO subsystem and the video subsystem. As a result of the deactivation of the system power off signal and the suspend control bits, the video subsystem enables normal refresh clock signals. The video memory and system memory are then switched to the normal fast refresh clock cycle.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a functional block diagram of a microprocessor system embodying the preferred embodiment of the present invention.

Figure 2 is a timing diagram of signals associated with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following description, for purposes of explanation and not limitation, specific register structures, mappings, bit assignments, etc. are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced in other embodiments that depart from these specific details. In other instances, detailed descriptions of well known aspects of microprocessor systems are omitted so as to not obscure the description of the present invention with unnecessary detail.

System Overview

The present invention is advantageously employed in a microprocessor design optimized for applications requiring low power consumption and compact size. Such applications particularly include small battery-powered personal computers of the types commonly referred to as laptops and notebooks. One preferred embodiment of such a microprocessor is briefly described below; however, it is to be understood that the present invention is not limited to this particular microprocessor design, and may be incorporated in virtually any processor design.

Referring to Figure 1, a preferred embodiment of the computer system 10 of the present invention is shown. In the preferred embodiment, computer system 10 includes a 386™SL Microprocessor manufactured by Intel Corporation, the corporate assignee of this invention. Such a computer system is compatible with the IBM™ PC AT Personal Computer. System 10 comprises three main processor components, designated as GENCPU 20, GENIO 30 and GENVGA 40. The combination of GENCPU 20 and GENIO 30 without the improvement disclosed herein are available from Intel Corporation under

a product designation of 386™SL Microprocessor SuperSet. GENCPU is an expanded central processing unit including a CPU, a memory controller, a cache controller, bus control logic and line buffers. A system memory 80 is coupled to GENCPU. System memory 80 substantially comprises dynamic random access memory (DRAM) devices. System DRAM requires a periodic refresh pulse in order to retain data. In normal operations of the computer system, this normal clock refresh pulse (i.e. first clock) is supplied to the system DRAM using a 16 MHz clock. System clock oscillator 21 for refreshing system DRAM 80 at a normal clock is also coupled to the GENCPU.

GENIO is a single chip input/output unit comprising parallel ports, dual serial ports, a real time clock unit, dual programmable interrupt controllers, dual programmable timers, dual DMA controllers and a memory mapper. GENIO also contains a register 31 denoted the PM_SUS_REF register. This register is used to command the GENIO to transition to the suspend mode. A bit in this register IO_SUS_REF is asserted by GENCPU 20 when suspend mode is requested. In addition, a suspend/resume signal 100 is received by GENIO. The suspend/resume signal 100 is used to request the power suspend mode on the occurrence of a hardware event. Such a hardware event may be a battery low condition, the expiration of a time-out timer, or the activation of a suspend/resume button on the computer case. For example, the action of opening or closing a lid on the computer case may activate the suspend/resume button.

In a suspend mode, GENIO provides two signals to system 10. The first signal 90 is a SYS_PWR_OFF signal. This signal indicates that the system 10 has transitioned to a power suspend mode. In response to this signal, other subsystems shut down non-vital components in order to conserve power. The second signal provided by GENIO is the REFREQ signal 91. This signal is the slow (32KHz) clock (i.e. second clock) used to refresh system DRAM 80 and video DRAM 50 during power suspend

mode. REFREQ 91 is therefore connected to GENCPU 20 and GENVGA 40 as shown if Figure 1. The details of the operation of these and other signals during suspend mode is described below.

GENVGA is a single chip graphics interface comprising a VGA graphics controller, video memory controller and flat panel display unit 60. Oscillator 71 for refreshing video DRAM 50 using a normal (48 MHz) clock is also coupled to the GENVGA. A video memory 50 is coupled to GENVGA. Video memory 50 substantially comprises DRAM devices. GENVGA also contains a register 41 denoted the PM_SUS_REF register. This register is used to command the GENVGA to transition to the suspend or resume mode. A bit in this register VGA_SUS_REF is asserted by GENCPU 20 when suspend mode is requested. In the preferred embodiment, the PM_SUS_REF register 31 in GENIO and the PM_SUS_REF register 41 in GENVGA are actually the same register. One register is a shadow of the other. In an alternative embodiment, there may be two separate registers, one in GENIO and the other in GENVGA. In either case, however, the two control bits in the PM_SUS_REF register, IO_SUS_REF and VGA_SUS_REF, are distinct and separate control bits. IO_SUS_REF is associated only with GENIO; VGA_SUS_REF is associated only with GENVGA. GENIO is able to sense when IO_SUS_REF transitions to an active or inactive state. GENVGA is able to sense when VGA_SUS_REF transitions to an active or inactive state.

All of the subsystems communicate with one another and with other system components (such as expansion slots, keyboard controller, disk controllers, etc.) via bus 11. In the preferred embodiment, bus 11 is an AT compatible bus. This type of bus is well known in the art.

Power Management

In the preferred embodiment, one function implemented by the present invention is a suspend/resume function. Suspend/resume

comprises a process wherein an internal or external event indicates to the computer system that it will be inactive for some extended period of time. For example, such an event may comprise an operator's action of closing the computer case or lid or it may comprise the expiration of an event timer. In response to the detected event, the computer selectively powers down to a low power consumption mode (i.e. power suspend mode). In response to a second event, such as the operator's opening of the computer case or lid, the computer system is automatically restored to the application program running at the time that the first event was detected.

Although the power management function is particularly useful for conserving power in a battery-powered computer system, it also has applications in desktop systems where power conservation is not a primary concern. In this regard, the process of bringing up and shutting down an operating system is often lengthy. The present invention allows an operator to turn "off" a computer system without shutting down the operating system. Likewise, the operator can turn the computer system "on" without having to go through the initialization process of the operating system.

In a variation of the suspend/resume function, a standby mode may be entered when the computer system is on but has remained idle for some predetermined period of time. When time-out occurs, an instruction or interrupt is invoked placing the system in a minimum power consumption mode. In response to an event, such as an operator action, the system is restored to the operating mode by the resume procedure.

Operation During Suspend Mode

In the preferred embodiment, the operation of the computer system is suspended on the occurrence of a hardware event, such as a battery low condition, the expiration of a time-out clock, or the activation of a suspend/resume button on the computer case. When a suspend event occurs, the GENIO subsystem 30 is the first subsystem to be notified of

the suspend request. This notification may occur as a result of an active SRBTN signal 100 as a result of the closure of the computer lid. The suspend notification may also occur internally to the GENIO as a result of the expiration of a time-out clock or a battery-low condition. In either case, a suspend request is activated in the GENIO subsystem 30. This suspend request is indicated by the rising edge 101 as shown in Figure 2.

As a result of the active suspend request, GENIO generates a power management interrupt (PMI) 92 to the GENCPU 20. The PMI 92 is transmitted to GENCPU 20 as shown in Figure 1. On receipt of the PMI, GENCPU saves the processing state of the system. This save operation includes saving the contents of system registers and stack pointers in a power management memory area. Saving the state of the system allows processing to resume normally after the power suspension period has been terminated and normal power has been restored. GENCPU 20 is then vectored to an interrupt processing routine containing program logic for handling the suspend request. One instruction in this programming logic is a suspend IO command.

After GENCPU 20 has saved the state of the system, GENCPU 20 begins to execute the program logic for handling the suspend request. As part of this sequence, GENCPU issues a write cycle (IOW) on bus 11 in order to set the suspend control bits IO_SUS_REF and VGA_SUS_REF to an active level. This IOW cycle is indicated by the falling edge 200 illustrated in Figure 2. In an alternative embodiment, two IOW cycles may be required if the PM_SUS_REF register 31 in the GENIO is a separate register from the PM_SUS_REF register 41 in the GENVGA. In the preferred embodiment, only one IOW cycle is required to activate both suspend control bits IO_SUS_REF and VGA_SUS_REF. The activation of these control bits is depicted by the rising edge 300 depicted in Figure 2.

Once the IO_SUS_REF and VGA_SUS_REF control bits are set by GENCPU 20, GENIO responds by asserting the SYS_PWR_OFF signal line 90 shown in Figure 1. The activation of SYS_PWR_OFF is shown by

the falling edge 400 shown in Figure 2. As a result of the active SYS_PWR_OFF signal, power to all peripheral devices and controllers is shut down with the exception of GENCPU, GENIO, GENVGA, system memory 80 and video memory 50. The pins connecting the GENIO, GENCPU, and GENVGA to the bus 11 are set to a tri-state condition which effectively disables communication over the bus 11. In addition, GENIO begins generating a slow (32 KHz) clock signal REFREQ 91 shown in Figure 1. A timing diagram 500 of the slow clock signal REFREQ is shown in Figure 2. REFREQ is received by both GENCPU and GENVGA.

As a result of the activation of suspend control bit VGA_SUS_REF, GENVGA interrupts the normal refresh video DRAM 50 by disabling the clock signals provided by oscillator 71. This action occurs at the rising edge 300 depicted in Figure 2. When GENVGA receives the active SYS_PWR_OFF signal 90 generated by GENIO while the VGA_SUS_REF bit is active, GENVGA begins to use the slow clock REFREQ to refresh video DRAM 50. The time between disabling normal refresh and enabling slow refresh is fast enough to not miss a refresh cycle. This slow refresh of video DRAM serves to substantially reduce the power consumption of the system while still preserving the contents of video DRAM. In an alternative embodiment, GENVGA does not use the VGA_SUS_REF bit to signal the switch to slow refresh. Instead, GENVGA delays for a time period after receiving the activated SYS_PWR_OFF signal. The delay required may be as much as 30 to 50 milliseconds. In the preferred embodiment, however, the combination of VGA_SUS_REF bit and the SYS_PWR_OFF signal provides a better implementation. After receiving the active SYS_PWR_OFF signal 90, GENVGA also disables its communication on bus 11 by setting its bus interface pins to a tri-state condition.

When GENCPU receives the active SYS_PWR_OFF signal 90 generated by GENIO, GENCPU begins to use the slow clock REFREQ

to refresh system DRAM 50. During the suspend mode, all logic other than the slow refresh of system DRAM and video DRAM and a suspend/resume state machine in GENIO is idle.

Operation During Resume Mode

The system 10 is in a power suspend state as long as the SYS_PWR_OFF signal is asserted. A hardware indication may be used to signal the termination of suspend mode and the resumption of normal operations. Such a signal may be denoted as a resume signal. A resume signal may be provided for a variety of reasons. In the preferred embodiment, a resume signal is generated mainly as a result of the opening of a cover on the computer. The opening of the computer cover causes a transition to occur on a switch operably coupled to the computer casing or the computer cover itself. In an alternative embodiment, a resume signal can be generated as a result of the computer user simply touching the keyboard or mouse device connected to the computer. In still another embodiment, a resume signal can be generated as a result of a ring detect signal received by a modem connected to the computer system 10. For any of these or other conceivable reasons, the user or system event signals the computer system that resumption of normal operations is desired.

A resume signal may be provided to the GENIO subsystem in the same manner that the suspend signal was provided as described above. Specifically, a suspend/resume signal line 100 is coupled to GENIO. A transition on the suspend/resume signal line 100 may be used to indicate either a suspend request or a resume request. In the preferred embodiment, a suspend request is indicated by a rising edge. This transition 101 is illustrated in Figure 2. Similarly, a resume request is indicated by a falling edge. Such a falling edge 600 is also shown in Figure 2. It will be apparent to those skilled in the art that the direction of the signal transition is immaterial to the operation of the present invention.

Equivalent embodiments of the present invention are conceivable where signals are either active high or active low.

Once GENIO receives a resume request on signal line 100, transition 600 occurs as shown in Figure 2. When this occurs, GENIO deactivates the SYS_PWR_OFF signal supplied generally to the system 10. This deactivation is depicted by edge 900 shown in Figure 2. GENIO then enables power to all system peripherals and controllers. Lastly, GENIO enables communication on bus 11 by removing the tri-state condition on the pins connecting the bus 11. Similarly, as a result of the deactivation of the SYS_PWR_OFF signal, GENVGA enables its communication on bus 11 by removing the tri-state condition on its pins connecting the bus 11.

Upon deactivation of the SYS_PWR_OFF signal, GENCPU is reset and vectored to processing logic for handling the resume request. This processing logic restores the system state previously saved in the power management memory area. The GENCPU interface to the bus is enabled by removing the tri-state condition on the interface pins. GENCPU then initiates another bus write cycle (IOW) for the purpose of resetting the IO_SUS_REF and VGA_SUS_REF control bits in the PM_SUS_REF register. This IOW cycle is depicted by edge 700 in Figure 2. The resulting reset of the IO_SUS_REF and VGA_SUS_REF bits is shown by edge 800 in Figure 2.

GENIO terminates the generation of the slow (32 KHz) refresh signal REFREQ 91 when the IO_SUS_REF bit is reset by GENCPU. The termination of the slow refresh clock is depicted by the final slow pulse 1000 in Figure 2.

Once GENVGA senses the deactivation of the VGA_SUS_REF bit while the SYS_PWR_OFF signal is also inactive, GENVGA enables its clock used for normal (48 MHz) video DRAM refresh. In an alternative embodiment, GENVGA does not use the VGA_SUS_REF bit to signal the switch to fast refresh. Instead, GENVGA delays for a time period after

receiving a deactivated SYS_PWR_OFF signal. In the preferred embodiment, however, the combination of VGA_SUS_REF bit and the SYS_PWR_OFF signal provides a better implementation. GENVGA then begins to refresh video DRAM 50 using the normal (48MHz) clock. Once the normal clock is active, GENCPU also begins to refresh system memory 80 using the normal (16 MHz) clock supplied by oscillator 21. Once DRAM is being refreshed using a faster clock, normal operation of the computer system 10 may be resumed.

It will be recognized that the above described invention may be embodied in other specific forms without departing from the spirit or essential characteristics of the disclosure. Thus, it is understood that the invention is not to be limited by the foregoing illustrative details, but rather is to be defined by the appended claims.

CLAIMS

What is claimed is:

1. In a computer system with a limited source of power, said computer system including a central processing unit (CPU) and dynamic memory, said dynamic memory being refreshed using a first clock, an improvement for conserving power comprising:

suspend mode detection means for generating a suspend signal upon the activation of a power suspend mode;

resume mode detection means for generating a resume signal upon the deactivation of said power suspend mode;

clock generation means for generating a second clock different from said first clock, said second clock being fast enough to be used to refresh said dynamic memory without causing the loss of data contained therein;

means for refreshing said dynamic memory using said second clock after said suspend signal is received from said suspend mode detection means; and

means for refreshing said dynamic memory using said first clock after said resume signal is received from said resume mode detection means.

2. The improved computer system of claim 1 wherein said computer system is battery powered.

3. The improved computer system of claim 1 wherein said dynamic memory is DRAM.

4. The improved computer system of claim 1 wherein said second clock is slower than said first clock.

5. The improved computer system of claim 1 wherein said suspend mode

detection means includes means for sensing an electrical signal applied to an external circuit pin.

6. The improved computer system of claim 1 wherein said resume mode detection means includes means for sensing an electrical signal applied to an external circuit pin.

7. The improved computer system of claim 1 wherein said suspend signal is generated upon a battery low condition.

8. The improved computer system of claim 1 wherein said suspend signal is generated upon receipt of a ring detect signal.

9. The improved computer system of claim 1 wherein said suspend signal is generated upon time-out of a timer.

10. The improved computer system of claim 1 wherein said suspend signal is generated upon operator action.

11. The improved computer system of claim 10 wherein said computer system is housed in a case and said operator action comprises closure of said case.

12. The improved computer system of claim 1 wherein said resume signal is generated upon operator action.

13. The improved computer system of claim 12 wherein said computer system is housed in a case and said operator action comprises opening of said case.

14. In a computer system with a limited source of power, said computer

system including a central processing unit (CPU) and dynamic memory, said dynamic memory being refreshed using a first clock, a process for conserving power comprising the steps of:

generating a suspend signal upon the activation of a power suspend mode;

generating a resume signal upon the deactivation of said power suspend mode;

generating a second clock different from said first clock, said second clock being fast enough to be used to refresh said dynamic memory without causing the loss of data contained therein;

refreshing said dynamic memory at said second clock after said suspend signal is received; and

refreshing said dynamic memory at said first clock after said resume signal is received.

15. The process of claim 14 wherein said computer system is battery powered.

16. The process of claim 14 wherein said dynamic memory is DRAM.

17. The process of claim 14 wherein said second clock is slower than said first clock.

18. The process of claim 14 wherein said generating a suspend signal step further includes sensing an electrical signal applied to an external circuit pin.

19. The process of claim 14 wherein said generating a resume signal step includes means for sensing an electrical signal applied to an external circuit pin.

20. The process of claim 14 wherein said suspend signal is generated upon a battery low condition.

21. The process of claim 14 wherein said suspend signal is generated is generated upon receipt of a ring detect signal.

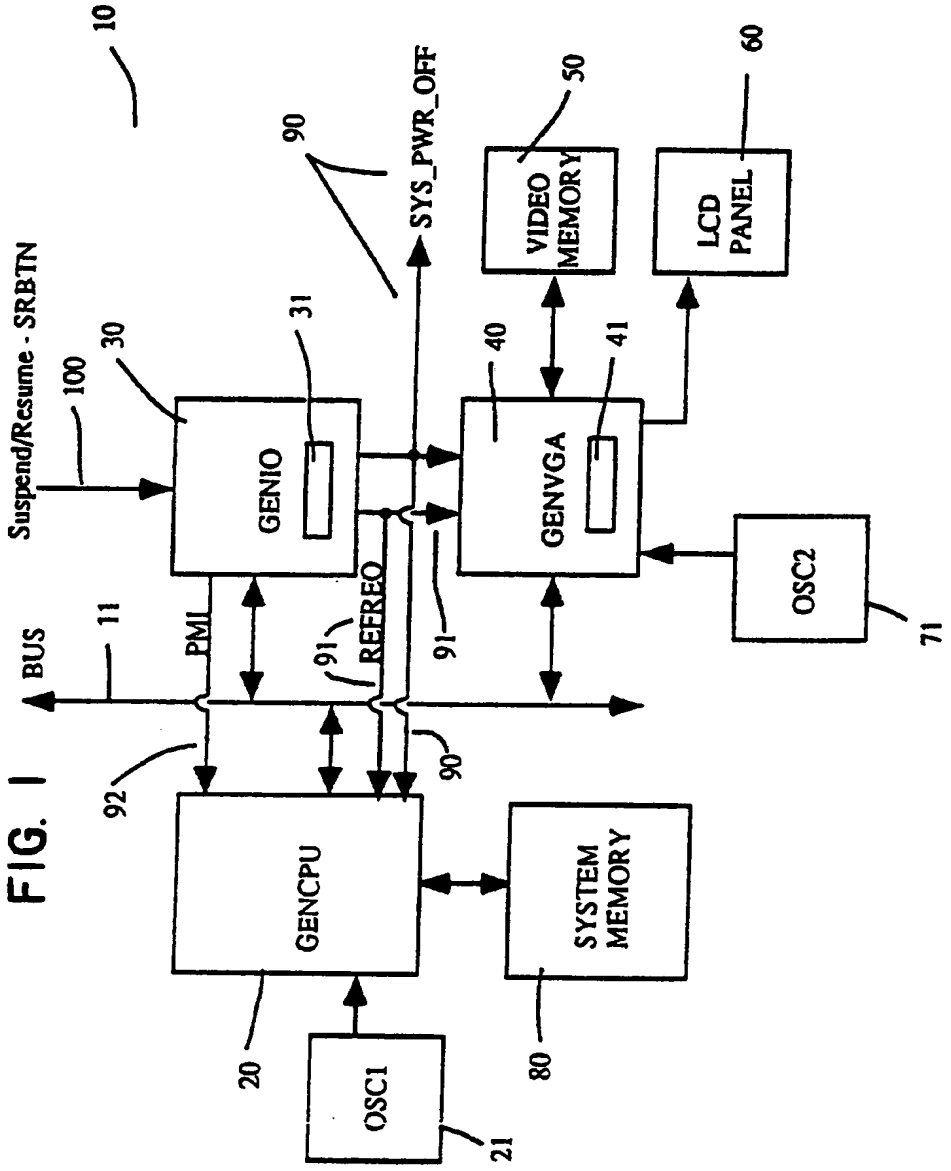
22. The process of claim 14 wherein said suspend signal is generated upon time-out of a timer.

23. The process of claim 14 wherein said suspend signal is generated upon operator action.

24. The process of claim 23 wherein said computer system is housed in a case and said operator action comprises closure of said case.

25. The process of claim 14 wherein said resume signal is generated upon operator action.

26. The process of claim 25 wherein said computer system is housed in a case and said operator action comprises opening of said case.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OSC1
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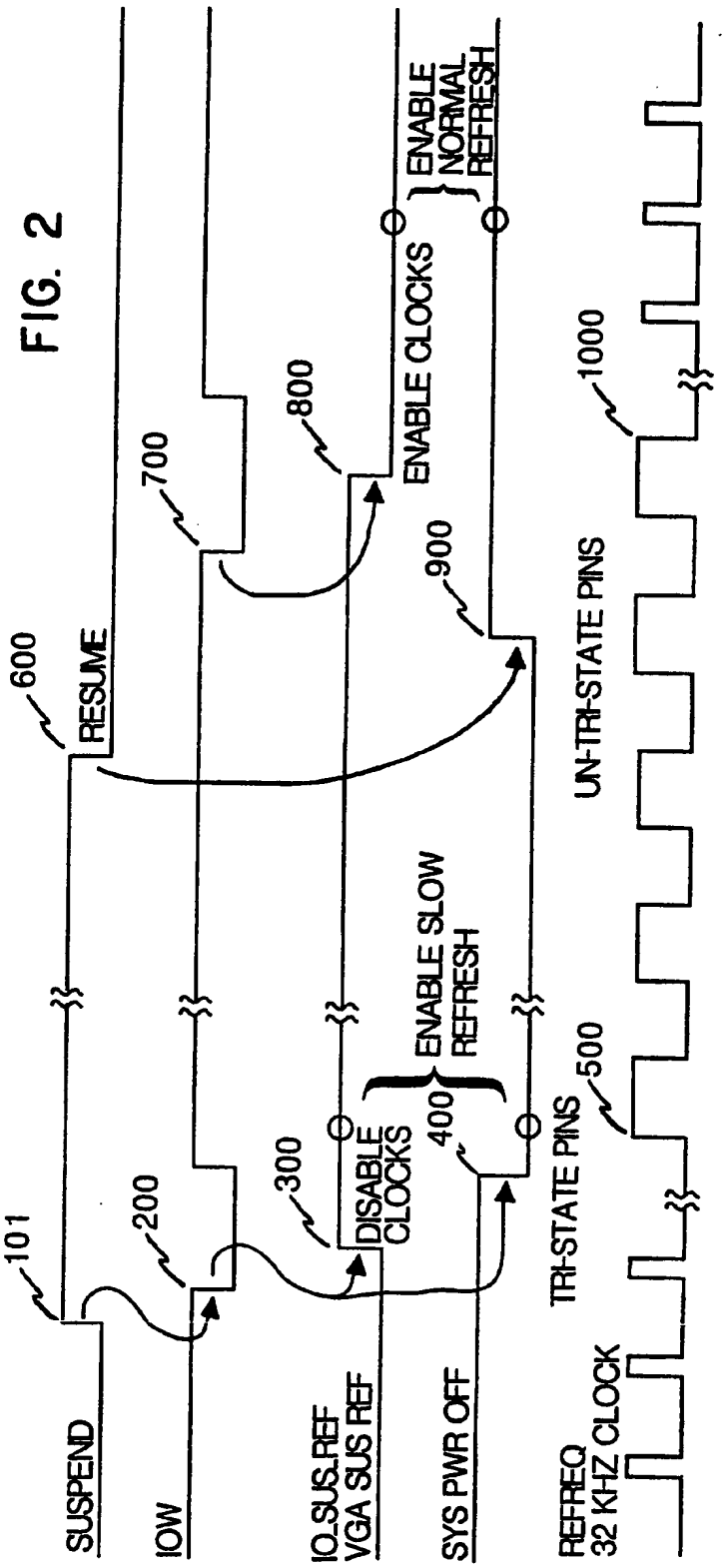
FIG. 1

FIG. 2


101
SUSPEND
200
IOW
300
DISABLE CLOCKS
IO.SUS.REF
VGA SUS REF
400
ENABLE SLOW REFRESH
SYS PWR OFF
500
TRI-STATE PINS
REFREQ
32 KHZ CLOCK
600
RESUME
700
800
ENABLE CLOCKS
ENABLE NORMAL REFRESH
900
1000
UN-TRI-STATE PINS

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US91/07597

I. CLASSIFICATI N OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(5) G06F 1/26, 1/32

U.S. CL. 395/750, 365/228, 365/222

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
U.S. CL	395/750, 365/228, 365/222

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X/Y	US,A, 4,686,386 (TADAO), 11 August, 1987, See fig. 1, column 2-4	1-10,12,14-20 23,25 / 8,9,13,21,22,24 25
Y	US, A, 4,137,563 (TSUNODA) 30 January 1979 (See fig 1)	1-26
Y	US, A, 4,698,748 (JUZSWIK ET AL) 06 October 1987 (See fig. 1, column 4-7)	8,9,11,13
Y	US, A, 4,570,219 (Shibukawa et al) 11 February 1986 (See fig. 3)	1-26
A	US,A, 4,893,271 (DAVIS ET AL) 09 January 1990, (See fig. 1)	1-26
Y	US,A, 4,615,005 (MAEJIMA ET AL) 30 September 1986 (See fig. 1)	1-26
Y	US,A, 4,901,283 (HANBURY ET AL) 13 February 1990 (See fig. 1)	1-26
Y	US,A, 4,851,987 (Day) 25, July 1989 (see fig. 1)	1-26

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
December 17, 1991	15 JAN 1992
International Searching Authority	**Signature of Authorized Officer**
ISA/US	MICHAEL R. FLEMING

Form PCT/ISA/210 (second sheet) (Rev.11-87)

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

Y	US,A, 4,907,150 (ARROYO ET AL) 06 March 1990 (See fig. 1)	1-26
A	US,A, 4,953,131 (PURDHAM ET AL) 28 August 1990 (See fig. 1)	1-26
A	US,A, 4,317,181 (TEZA ET AL) 23 February 1982 (See Fig. 3, column 3-9)	1-26
Y,P	US,A, 5,041,964 (COLE ET AL) 20 August 1991 (See fig.1	1-26
A	US,A, 4,207,142 (BAKER ET AL) 17 November (See fig. 1)	1-26

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers . . because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers . . . . . , because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

3. ☐ Claim numbers_____, because they are dependent claims not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [2]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.